Intel® 820 Chipset

A Revolutionary Architecture for Mainstream Performance PCs in 2000

Introduction

The PC and the Internet are mutually dependent—advances in one technology will require mirrored advances in the other. Advances in the Internet deliver higher bandwidth and more functions to businesses and consumers, while advances in the PC allow users to take better advantage of restricted bandwidth and complete electronic transactions of all kinds in a secure environment. For commercial users, the Intel® 820 chipset offers new manageability and security features, and headroom for next-generation operating systems, applications and processors. Consumers gain the ability to run dramatically richer graphics and multimedia content on a platform that can accommodate future advances in processor technology.

The 820 chipset enables platforms that can scale with technology advances in the Intel® Pentium® III processor product family, allowing users to capitalize on the benefits of the Internet. It achieves these goals through the introduction of two major new technologies, AGP4x and Direct Rambus memory, which double bandwidth in the critical areas of graphics and memory, respectively.

Intel has five major initiatives reflected in the 820 chipset.

Stable platforms allow IT managers to deploy large numbers of systems that run an identical software image. The 820 chipset's Intel® Hub Architecture allows Intel to enhance and update components of the chipset without necessarily forcing new system images into the installed base. Coupled with stabilized device drivers, this initiative will allow IT managers to plan systems for deployment over a period of 12 months or greater.

Constant computing reflects the ability of a platform to perform multiple functions in the background without compromising foreground performance. These background tasks can perform continuous virus checks, compress and decompress network traffic for more effective use of bandwidth, scan the hard drive for problem areas and automatically repair defects. The 820 chipset architecture, along with Direct RDRAM* memory, can support multiple simultaneous memory access threads without penalty.

Rich content delivery allows users and content providers to interact more effectively over the constrained bandwidth of the Internet. Initially, compression and decompression technologies will be the primary features, but 3D object modeling can deliver dramatically reduced bandwidth and increased quality, as long as the processor can render the objects in acceptable time. In the 820 chipset, the introduction of RDRAM and AGP4x provide the local processing bandwidth to deliver outstanding 3D graphics.

Platform security provides the hardware foundation for software security technologies that will eliminate concerns about privacy and security in electronic transactions. These advances will greatly reduce the risks for all electronic commerce participants, including banks, buyers, sellers, corporations and individuals. The PC and the Internet will provide the medium for greatly accelerated business processes, ultimately with lower risk than paper-based systems. The firmware hub in the 820 chipset implements a random number generator (RNG), the first hardware-based security enhancement in the Intel® platform.

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Manageability is enhanced by the Alert-on-LAN (AOL) feature, which allows the PC to report its status to the network controller, even if it is incapable of booting due to hardware or software error. The chipset has watchdog timers that can detect and restart a hung system without user intervention. The 820 chipset also provides improved sleep and wake features, supporting the Instant-On specification, for improved power management and better acceptance of the always-on PC.

The Intel 820 Chipset and System Manufacturers

The 820 chipset represents Intel's strategic platform for 2000 and will be introduced in the fourth quarter of 1999, with shipments continuing well into 2001. System manufacturers will find that its enhanced buses and feature set lead to more-robust designs that can extract the full performance of Intel's Pentium III processor. The AGP4x interface, with its 1GB/sec bandwidth, in conjunction with the 1.6GB/sec of main memory bandwidth and the advanced SIMD and streaming instructions of the Pentium III processor, opens up new vistas of graphics performance for applications formerly constrained to run on workstation-class products.

Intel recommends that manufacturers develop a modular BIOS that allows for minor changes in system features without a mandatory update to the user's system image. This approach is critical to delivering stable platforms to commercial buyers.

The Intel 820 Chipset and Business Users

For commercial users, the 820 chipset represents the platform of choice for deployment starting late in 1999. It has performance headroom to accommodate processor performance advances well into 2001, and its initial deployment to advanced users can be followed up by broad deployment to all users before the second half of 2000. IT managers will be able to build a substantial base of machines built on this platform, reducing the complexity of system management while benefiting from the new features, advanced performance and flexibility of the 820 chipset architecture. The new hub and low pin count (LPC) interface architectures allow Intel to enhance the feature set on a rolling basis without affecting the system image, allowing IT managers to stabilize their platforms over an extended period of time.

The Intel 820 Chipset and Windows* 2000

Windows 2000 is a major advance in operating system technology, bringing a new measure of stability, security, flexibility and functionality to the PC. The 820 chipset, in conjunction with the Pentium III processor, will deliver the power to support this new operating system, its advanced features and its derivatives, providing investment protection for IT managers. Of particular note is the platform bandwidth and performance to support the encrypted file systems and encrypted network connections expected in Windows 2000.

The Intel 820 Chipset and Graphics Users

The 820 chipset deserves special mention for commercial users involved in the processing of still or moving images. The systemwide increase in bandwidth that it introduces, with particular emphasis on AGP4x and Ultra ATA 66, will enable graphics users to complete image editing tasks in less time than before and to handle larger, higher-resolution images. With a second processor and multithreaded applications such as Photoshop, the 820 chipset platform can provide workstation-class performance for these applications at a conventional desktop price.

The Intel 820 Chipset and Consumers

Consumers will find that the high bandwidth of the 820 chipset and its subsystems unlocks the full performance of the Pentium III processor, enhancing multimedia applications, such as digital photograph editing and processing, video editing, and entertainment applications. The advanced power management features will allow the platform to support the Instant-On specification, enabling consumers to take full advantage of the burgeoning availability of full-time, high-speed Internet access from DSL and cable modem providers. The platform's security features will further enhance the privacy and security of Internet commerce through the RNG. This feature allows consumers to select truly random cryptographic keys at ease, eliminating the concern that a weak key might inadvertently be selected. In conjunction with good encryption algorithms, these strong keys can help secure the privacy of an Internet conversation.

The 820 Chipset: *Overview and Siblings*

The 820 chipset represents Intel's major platform initiative for system products that will ship throughout 2000, with expected shipments well into 2001. It is designed to be the platform of choice for the Pentium III processor architecture, supporting the higher-bus bandwidths and clock frequencies that this processor will deliver over its predecessor, the Intel® Pentium® II processor. The 820 chipset is part of a family of chipsets that will support all desktop computing market needs in 2000: the Intel® 810E chipset, for mainstream systems where cost is a primary factor; the 820 chipset, for mainstream performance systems and where a long platform life is desirable; and

the Intel® 840 chipset, for workstation applications. Table 1 shows the relationships between these three chipsets. These chipsets also share the same firmware hub and I/O controller hub, an important factor in delivering consistent and stable platforms. This architecture allows the 800 series of Intel chipsets to be modified, enhanced and expanded without creating major discontinuities in software support.

Table 1. Intel's new platform chipsets

Chipset	Intel® 810E chipset	Intel® 820 chipset	Intel® 840 chipset
System cost	Low	Mainstream/Performance	Premium
Defining features	Integrated graphics; cost	Performance; platform longevity and stability	Workstation
Maximum processors	1	2	2
Memory	100MHz SDRAM (PC100)	1 RDRAM channel (PC600/PC700/PC800)	2 RDRAM channels (PC600/800)
Target processor	Intel® Celeron™ Processor	Pentium III processor (1 or 2)	Intel® Pentium® III Xeon™ processor (1 or 2)
	Intel® Pentium® III processor		Pentium III processor (1 or 2)

The Intel 820 chipset embodies a plethora of technology advances, enhancing management features over previous chipsets, doubling most interface bandwidths, delivering performance headroom for future processors and implementing the first platform hardware security features. The chipset also embodies a new interconnect architecture, transitioning the PCI bus to a peripheral role in favor of the use of high-speed low pin count buses. This new architecture has double the aggregate bandwidth of its predecessor, the Intel® 440BX chipset, in every critical area. It also supports the 133MHz processor system bus (PSB) introduced on the Pentium III processor. The Pentium III processor has an enhanced bus interface and is capable of fully exploiting this bandwidth.

Technology Background

To understand the 820 chipset, it is helpful to understand the two major challenges facing system designers today: electrical integrity and system bandwidth. This section gives a background on each of these issues and sets the stage for understanding the advanced bus technologies implemented in the 820 chipset.

Electrical Design Challenges

An electrical pulse traveling down a wire is a complex phenomenon. James Clerk Maxwell derived a set of equations in the late 19th century that so effectively modeled and predicted the behavior of electrical signals that he was able to predict the existence of radio waves. These equations exposed the essential duality of electrical signals: some travel inside the conductor, some travel outside of it. Depending on the physical dimensions of the conductor and the rate of change of the signals, more or less energy will be distributed outside of the conductor. If this energy is able to transfer to other circuits, or is not properly controlled inside its own circuit, signal integrity can be lost and reliability is compromised.

As this problem scales with higher frequencies, higher currents, complex layouts and more conductors, the solutions are clear: lower voltages and hence lower currents, fewer conductors, simpler circuit paths, and advanced design and simulation practices. Using fewer conductors brings a double benefit: less energy can escape and the circuit paths become considerably simpler. The 820 chipset incorporates four such highly controlled circuits, or buses: the Processor System Bus (PSB), the Direct Rambus memory interface, AGP4x and the hub interface. The LPC interconnect bus, while not in the same bandwidth category of these other buses, benefits from pin count reduction techniques. These buses are easily scaled by advancing their clock frequencies, while their physical simplicity reduces the design challenge. In the future, new high-speed serial buses such as next generation I/O and USB 2.0 will displace other parallel buses in the system, further reducing complexity and enhancing system integrity. Table 2 shows the performance of the buses in the 820 chipset and, where applicable, significant electrical integrity features.

Table 2. Bus performance and integrity features

	Bandwidth	Effective transfer rate	Type	Feature
Processor System Bus	1GB/sec	133MHz	Multidrop	GTL+
Direct Rambus	1.6GB/sec	400MHz	Controlled bus	Low voltage
AGP4x	1GB/sec	133MHz	Point-to-point	Low voltage
Hub interface	266MB/sec	266MHz	Point-to-point	Active matching
LPC	4MB/sec	33MHz	Multidrop	

Electrical Integrity: Summary

In summary, the 820 chipset incorporates the following advances to contain the challenges of Maxwell's equations:

- Hub interface, a reduced pin count high-integrity bus for system interconnect
- Direct Rambus for memory interconnect
- Advanced cabling for ATA-66 hard drive interconnect
- A new 1.5V signal level for AGP4x.

These enhancements increase reliability and performance while lowering system cost. Designers are cautioned, however, that these buses are unforgiving of layout deficiencies and must be handled with respect. Intel's 820 chipset application note provides full layout design details for these new buses.

The Bandwidth Challenge

As processor technology advances, both clock rates and work performed per clock cycle will increase. These advances in processor performance demand increased performance through the entire system if the full processor performance is to be realized. Table 3 shows how the 820 chipset outperforms its predecessor, the Intel 440BX chipset, in available bandwidth through every major interface.

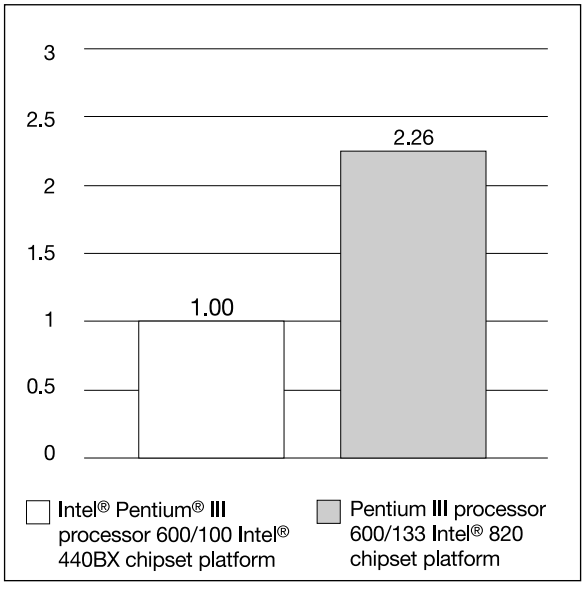
Table 3. System bandwidth comparison: Intel 820® chipset vs. Intel® 440BX chipset

	Intel® 440BX chipset	MB/sec	Intel® 820 chipset	MB/sec
PSB	Intel® Pentium® II processor 66–100	512–768	Intel® Pentium® III processor 133	1,024
Graphics	AGP2x	533	AGP4x	1,066
Memory	100MHz SDRAM	800	DRDRAM	1,600
Bridge bus	PCI	133	Hub interface	266
HDD	ATA-33	33	ATA-66	66

Validating Bandwidth Headroom

Intel has developed a synthetic benchmark, the Platform Bandwidth Test, that tests the memory bandwidth available to the system; the test is available on CD-ROM or from Intel's Web site. The test code uses the Streaming SIMD Enhancements (SSE) to transfer a total of about 2GB of processor reads, 2GB of processor writes, and 6GB of AGP transfers from main memory. The test, in addition to reads and writes, performs operations that simulate 3D rendering. The overall effect is to simulate the large volumes of memory and system traffic expected from next-generation applications. Figure 1 shows the relative results of this test when run on the Intel 440BX chipset platform and the Intel 820 chipset platform.

Figure 1: Intel® Platform Bandwidth Test



The test shows an increase in aggregate bandwidth of 126 percent. This test clearly demonstrates that the Intel 820 chipset architecture has significant headroom to accommodate future performance enhancements and new applications.

Low Pin Count Buses

The 820 chipset introduces three reduced pin count buses that increase data transfer rates through the use of narrower buses but higher-speed, scalable clocks. The first of these is the Direct Rambus interface, a new memory interface that adds up to 1.6GB/sec of memory bandwidth in a 33-pin bus.

The second is the hub interface, which replaces the PCI bus as the internal interconnect between the core logic and the internal system peripherals. It delivers 266MB/sec in a one-pin bus. The hub interface is a point-to-point bus with a monitoring signal line to closely match the signal characteristics to the circuit board layout. It uses eight data lines, two lines for a differential strobe, three lines for protocol control and two lines for signal integrity. There is an optional parity signal for applications that require it, but the bus is designed for totally reliable data transfer. The strobe signal clocks at up to 133MHz per second and transfers data at 266MB/sec through the use of both clock edges. The PCI bus is now relegated to a peripheral interface in the I/O controller hub and is removed from the bandwidth-critical core of the system.

The final interface is the LPC bus, which provides the interface to a controller that supports traditional ISA peripherals including serial, parallel, game and floppy ports, through a seven-pin interface (four data, typically three control). The LPC interface also provides the electrical connection for the firmware hub interface, which supports the BIOS flash memory and the RNG function.

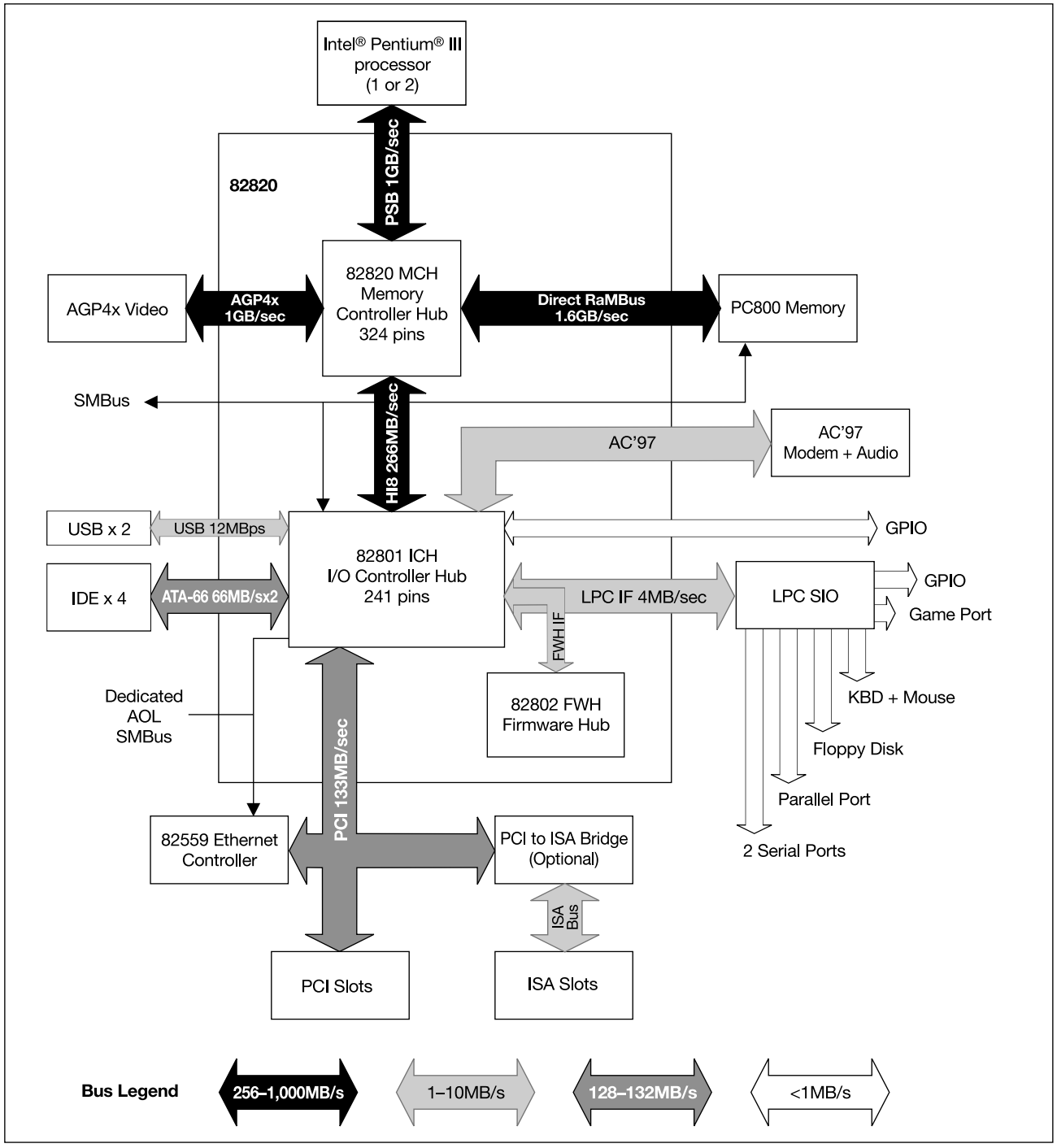
The Intel 820 Chipset Architecture

Intel's new 820 chipset consists of three components: a memory controller hub (MCH, 82820), an I/O controller hub (ICH, 82801), and a firmware hub (FWH, 82802). It will commonly be used with an LPC super I/O part and possibly also with a PCI to ISA bridge. The chipset takes its name from the memory controller hub, but shares a common firmware hub and I/O controller hub with its contemporaries (see Figure 2).

This commonality of system components guarantees that the new chipsets share identical software for features and enhancements implemented in these peripheral devices, and reduce development, implementation and support costs. The hub architecture, with its narrow, high-speed buses, also saves pins. The 820 chipset has a total of 565 pins between its two major components, compared with 816 on the 440BX chipset. This reduction in pin count brings with it a reduction in manufacturing cost and increased reliability.

Figure 2 shows the Intel 820 chipset system architecture in its entirety.

Figure 2. The Intel® 820 chipset system architecture



Intel® Hub Architecture

The Intel® Hub Architecture partitions the system into three major components. It is distinguished by its use of a very high bandwidth (266MB/sec), reduced pin count interface known as the hub interface (HI8 in the 820 chipset). HI8 implements this bandwidth of 266MB/sec—double that of PCI—in just 16 pins, eight of which carry data. The interface can be scaled in both width and clock frequency. Its bandwidth and architecture allows the chipset to deal effectively with isochronous data without the bottlenecks associated with the PCI protocols. This bandwidth is achieved through the use of very high clock rates, differential signaling on the strobe line, a reference voltage signal that provides reliable switching and a compensation signal that allows the chip to match its buffer characteristics to those of the printed circuit board. The bus is source-synchronous—the clock and data are driven at the source, ensuring synchronous arrival. The combination of source-synchronous clocking and the voltage

and matching signals guarantees electrical integrity, but a parity option is available for those applications that require signal checking throughout the system, such as high-integrity servers. This option is not implemented on the 820 chipset. The interface signals and their functions

Table 4. Hub interface 8-pin count

Function	Pins	Comment
Data bits	8	
Strobe	2	Differential signal supports 266MHz transfer rate
Control	3	Includes optional (not implemented in 820) parity signal
Trace matching	1	Matches signals to circuit board
Hubref	1	Signal voltage reference

are shown in Table 4.

The memory controller hub incorporates the memory controller, the hub interface, the AGP4x interface and the processor system bus interface. The I/O controller hub incorporates a hub interface, the PCI interface, the USB controller, the ATA-66 controller, the AC'97 controller, and LPC interfaces for the firmware hub and legacy I/O. The firmware hub incorporates the BIOS flash memory and the RNG.

Traditional PC I/O functions, including legacy serial and parallel I/O, the floppy interface and the game port, are supported by a super I/O part with an LPC bus interface. The ISA interface has been eliminated from the system logic and can instead be supported by an optional PCI-to-ISA bridge. However, Intel recommends against general support for the ISA bus to improve system compatibility, reliability, manageability, performance and cost.

The 82820 Memory Controller Hub

The MCH is the heart of the system, linking all of the major components—processor, graphics, memory and I/O—together through high-performance buses. It has an aggregate bandwidth of 3.9GB/sec and its multipath concurrent internal design permits peak transfer rates of 1.9GB/sec.

Accelerated Graphics Port 4x (AGP4x)

The AGP architecture was developed to address the ever-increasing bandwidth needs of graphics accelerators. The initial implementation, AGP2x, delivered double the bandwidth of PCI. Consequently, it had to connect directly to the memory controller to avoid overload of the PCI bus. AGP4x brings with it transfer rates in excess of 1GB/sec. This additional bandwidth demands a corresponding increase in main memory bandwidth, delivered by the use of the 1.6GB/sec Direct Rambus interface. In conjunction with the Pentium III processor, the 820 chipset opens up new opportunities for advanced graphics systems.

The higher bandwidth of AGP4x brings with it the electrical challenges described in this document. The solution is a change in the interface voltage to 1.5V, down from the 3.3V used in AGP2x. To provide compatibility with AGP2x components, AGP4x incorporates intelligent buffer technology, which senses and selects the correct signaling voltage for the interface.

Direct Rambus DRAM (DRDRAM)

Dynamic memory has a long history, pioneered by Intel in the 1970s. Even then, memory capacity advanced at such a rate that it soon became clear that direct addressing of the memory capacity of a single device demanded more pins than necessary, driving up chip and system packaging costs. The architecture of DRAM is such that it is sensible to provide the address in two successive words—the row address and the column address—reducing the pin count of the package and the complexity of the circuit board in exchange for a trivial increase in controller cost. Therefore, DRAMs have historically received two address inputs and returned one data output.

In the late 1980s, microprocessors began to outpace the transfer rate of DRAMs, so the architecture evolved. First came fast page mode, in which the memory controller uses just one row address, but provides multiple column addresses to extract the data from memory. Next came EDO, in which the DRAM accepts the next column address before it provides the data from the previous request. This overlapping allows a doubling in the DRAM transfer rate. Then came synchronous DRAM, which provides an address then extracts successive memory locations through the application of a clock, eliminating the circuit noise and timing overhead of providing incremental addresses to the memory (the memory incorporates a counter that allows it to generate its own column addresses). Over this period, system designers widened up the memory data path to 64 bits to transfer eight bytes at a time, yielding a peak transfer rate of 800MB/sec with 100MHz synchronous DRAM. Further advances in memory speed are possible: designers are showing 133MHz SDRAM systems, and memory manufacturers are working on using both edges of the clock to double the transfer speed. However, Maxwell's equations erect a barrier at these speeds, demanding expensive circuit board designs to transfer 64 bits of data

through connectors and traces without compromising reliability. Furthermore, the need for increased bandwidth demands wide buses, but increasing memory densities force memory arrays to become too large. These are the fundamental reasons why SDRAM must yield to Direct Rambus in high-performance systems.

The Direct Rambus interface represents a new approach to memory interfacing. The 12 address bits, 4 control bits and 64 data bits of a conventional memory array are replaced by a single 16-bit bidirectional bus, clocked on both edges of a high-speed 400MHz clock and providing maximum data transfer rates of 1.6GB/sec per device. The bus now carries commands to the memory, and transfers data in both directions in response to these commands. The lower pin count of the Rambus interface allows designers to accept a more challenging electrical design task in exchange for relatively simple, easily-manufactured designs that can deliver high data rates with a minimum component count. The low pin count allows channels to be easily added to a controller, providing a practical method to scale bandwidth for several generations of chipsets.

Initial Direct Rambus memory modules will be available with transfer rates of 600, 700 and 800MHz and will be designated as PC600, PC700 and PC800 memory respectively. These three performance points will enable system and memory manufacturers to better optimize performance, yield and cost.

The 82802 Firmware Hub (FWH)

The firmware hub incorporates system features that have no external interface. In the 82802, this category includes the flash memory and the random number generator (RNG). The FWH has its own unique protocol, but shares the LPC bus interface pins to connect to the I/O controller hub. This multiplexing approach reduces system pin count and complexity.

Flash Memory

The firmware hub provides the boot flash memory for the system, and is available in both 4Mb (512KB) and 8Mb (1MB) configurations. The larger size provides for integrated BIOS designs and offers the opportunity to perform sophisticated preboot management, diagnostic and security functions.

The Intel® Random Number Generator (RNG)

One of the great challenges to any secure system is the proper generation of keys. For example, an encryption system that uses a 40-bit key (the largest key currently permitted under most export control laws) can be cracked in a matter of hours on a modern PC. By contrast, the 56-bit key used in DES takes decades of effort on a single PC and a 128-bit key is beyond the bounds of all known or projected technology advances.

However, the security of a 128-bit cipher can be completely negated by the selection of an overly simple key. For example, English text has an effective key length of about 1.4 bits per character. Therefore, a 20-character passphrase is equivalent to a 28-bit key and easily cracked by a personal computer. It is extremely difficult for a human to produce sufficient randomness to realize the protection of a 128-bit key. Furthermore, software RNGs suffer the same problem. Algorithms that use the time of day, the date, and any other system variables available to them still fall far, far short of even generating a secure 56-bit key.

Therefore, the 820 chipset firmware hub incorporates a hardware RNG. The device uses thermal noise in a semiconductor junction to produce random circuit transitions. These transitions are aggregated and checked for true randomness, then assembled into a random key of any desired length. A software driver can use this hardware to deliver truly random bitstreams to security applications, guaranteeing that security will not be compromised because of the selection of a weak key and that users can have truly private conversations.

The 82801AA I/O Controller Hub (ICH)

The 82801AA ICH performs the functions previously embodied in the south bridge. However, the higher bandwidth of the hub interface allows the hub to offer dramatically increased performance. This is particularly important in the areas of the ATA-66 interface, which would otherwise consume all traditional PCI bus bandwidth, and the AC’97 and USB interfaces, which require controlled response times and throughput to deliver uninterrupted audio and modem connections, and other features, to the user.

Alert on LAN (AOL)

Current manageability solutions provide great insights into the state of a functional PC, but do not address the case of a PC that is unable to boot. The 820 chipset allows even a nonbooting machine to report basic status to a network management host. It achieves this through its AOL feature, which implements processor-independent state machines that can report status data to the network administrator even if the processor is incapacitated. This data is reported over a dedicated unidirectional SMBus interface, a low-speed serial bus for power management and low-level control and reporting

functions. Future chipsets will use a bidirectional interface to support AOL 2.0, conferring on the PC the ability to power up in response to a remote command. The 820 chipset requires an Intel® 82559 network controller (or compatible product) to provide the AOL service. It is expected that other manufacturers will incorporate the technology into their controllers. The ICH and the 82559 incorporate simple state machine devices capable of reporting system hardware status to a predefined host address with no processor intervention. The information includes relevant hardware management bits stored in the 820 chipset:

- Chassis intrusion
- Processor not present
- Custom messages
- Watchdog timer
- Thermal event monitor.

Chassis Intrusion

By means of an optional sensor—mechanical, or optical, or both—connected to the chassis, the ICH can detect and remember the opening of the system cover. This function operates even when the system is disconnected from the power supply. The function is valuable to system administrators as it announces that the system might have been subjected to tampering. Such tampering would include the installation of unauthorized or unapproved peripherals, or removal or substitution of the processor, memory or hard drive.

Processor Not Present

The ICH monitors processor activity and can detect when the processor stops or fails to fetch its first instruction. The AOL interface can report this status to the network administrator.

Custom Messages

The ICH incorporates a message register that is reported to the AOL interface during the boot process. The BIOS can set bits in the register to report boot status across the network.

Watchdog Timer

The watchdog timer restarts the processor in the event of a system crash. This event can be reported to the network administrator, alerting the possibility of system problems.

Thermal Event Monitor

The ICH supports a single thermal event monitor signal. If this signal trips, it can report to the administrator. Often, system failures are caused by thermal problems inside the machine or in its environment. This feature can aid in identifying such issues. An example is an air-conditioning system that fails on a hot day, causing unidentifiable system failures.

ATA-66

The high-end hard drives shipping in 1999 achieve a data transfer rate from the media to the head of approximately 33MB/sec, or (after error correction and adjustment for track-to-track seek time) about 33MB/sec. This transfer rate represents the maximum sustained rate that the drive can deliver to the system, although its burst rate may be higher because of on-board caches. The ATA-33 interface can handle this data rate, but hard drives will catch up with the interface and should exceed it in mid-1999. Therefore, a higher performance interface is required to avoid throttling system performance because of a limited data transfer rate to the hard drive. Note that ATA-33 added error detection and correction to the interface, greatly reducing the risk of data corruption at these high transfer rates.

ATA-66 is a natural extension to the existing high-speed ATA-33 hard disk drive interface. Transferring two bytes of data per clock edge, four bytes per clock, it is capable of maximum sustained burst transfer rates of 66MB/sec. Achieving these high-speed data rates is a challenge to the electrical design of the system, a problem solved by the addition of 40 ground wires to the existing 40-wire IDE cable. Therefore, ATA-66 systems use 80-wire cable with 40-pin connectors. Substituting these cables with regular IDE cables will potentially result in degraded performance because of the excessive errors that a regular IDE cable could induce. Users and manufacturers should be aware of this problem.

AC'97

AC'97 is a new audio interface designed to improve cost, quality and stability of the PC audio subsystem. The ICH incorporates the digital component of the AC'97 interface.

The key electrical feature of the AC'97 architecture is the divorce of the analog and digital subsystems. This separation dramatically reduces digital noise in the analog subsystem and enables the use of low-cost, high-quality CODECs. All of the analog data is passed over a five-wire serial bus that uses time division multiplexing. There are three control channels and up to nine 20-bit audio/modem slots available in each direction at a sampling frequency of up to 48kHz. Each slot represents one high-quality mono audio or modem channel. The ICH implements two audio input channels, two audio output channels, a mono microphone channel and a bi-directional modem channel for a total of seven slots.

This arrangement provides two significant advantages. First, the only digital signals in the area of the part are the five serial interface lines (data in, data out, sync., a 12.88MHz clock and reset). Therefore, there is much less digital noise to deal with and the system can deliver a high-fidelity 90dB signal-to-noise ratio. Secondly, the simple interface allows nine audio channels to be managed across just five pins. This capacity allows the CODEC to address most conceivable (and all reasonable) audio configurations.

The audio modem riser (AMR) feature takes advantage of the low pin count to enable manufacturers to implement the modem, and possibly the audio as well, on an inexpensive riser card. The AMR approach allows the designer considerable flexibility in the implementation of an internal modem to accommodate international regulatory standards, without affecting the audio subsystem.

PCI Bus Interface

The PCI bus is supported in the ICH. Unlike previous chipset designs, the PCI bus is no longer central to the system and is not used in the internal datapaths. Although PCI has served the PC architecture well, its bandwidth is no longer sufficient to support the high performance of the PC system core. However, many peripheral devices are available on PCI and it will continue to be the bus of choice for many peripherals and traditional card-based expansion. In the 820 chipset architecture, the PCI bus is the only option for supporting network interfaces.

Legacy I/O and USB

The traditional dual serial ports, parallel port, game port, and keyboard and mouse ports are all supported in the super I/O controller chip. In the 820 chipset architecture, this chip interfaces via the LPC bus, rather than the traditional ISA bus. The reduced pin count of the LPC bus enables the controller to have more pins allocated to interface functions, or to be housed in a lower-cost package.

SMBus and GPIO

There are two additional components worthy of mention. The SMBus interface made its desktop debut in the Intel® 430TX chipset. In the 820 chipset, it is used to extract RDRAM control information; a second, dedicated SMBus channel passes AOL information to the Ethernet controller. Original equipment manufacturers (OEMs) can use the SMBus to add other features to the platform. Power control and platform management features are targets for this interface.

The 820 chipset provides two sets of general purpose I/O, one from the ICH and one (optional) from the LPC super I/O device. These signals provide a handful of general-purpose control lines that can be used by the OEM to differentiate its products.

Conclusion

In summary, the Intel 820 chipset provides bandwidth and headroom to support a new generation of productivity applications, and offers substantial performance gains on media-rich applications today.

For more information, visit the Intel Web site at: developer.intel.com

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